

Abstract of the Disclosure

A method for testing a multi-chip package formed of different types of semiconductor devices, using an integrated burn-in test program which can reduce throughput time, reduce the possibility of error by an operator, and reduce workload. A multi-chip package is tested in burn-in equipment capable of applying a plurality of scan control clock signals. An integrated burn-in test program requires fewer burn-in test programs to be uploaded, fewer contact tests, and fewer bin sorting operations.